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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,077	08/24/2001	Garnett , Paul Jeffrey	5681-03100	4242

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,077	JEFFREY ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1 and 3-25 are presented for examination. This office action is in response to the RCE filed on 8/19/04.

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Bannon et al. (Bannon) U.S. Patent No. 5,987,544.

As to claim 1, *Bannon* discloses the invention as claimed. Bannon discloses a dirty memory subsystem for a computer system, the dirty memory subsystem comprising storage operable to store redundant copies of dirty indicators (abstract lines 8-11, "duplicate tag", col. 4 lines 42-47, and col. 6 lines 46-49, "two identical copies" read on this limitation), each dirty indicator being associated with a respective block of main memory and being settable to a predetermined state to indicate that the block of main memory associated therewith has been dirtied (col. 2 lines 32-39) and a control logic (Fig. 2 Ref 15a) operable to read the redundant copies (Fig. 2 ref. 28) of a dirty indicator from storage and to treat the block of memory associated therewith as dirtied if

at least one of the redundant copies of the dirty indicator has the predetermined state (abstract, dirty bits on Dtag reads on this limitation).

As to claim 12, *Bannon* discloses the invention as claimed. Bannon discloses a computer system comprising a dirty memory subsystem and at least one processing set that includes main memory, the dirty memory subsystem comprising storage operable to store redundant copies of dirty indicators (abstract lines 8-11, "duplicate tag", col. 4 lines 42-47, and col. 6 lines 46-49, "two identical copies" read on this limitation), each dirty indicator being associated with a respective block of main memory and being settable to a predetermined state to indicate that the block of main memory associated therewith has been dirtied (col. 2 lines 32-39) and a control logic (Fig. 2 Ref 15a) operable to read the redundant copies (Fig. 2 Ref. 28) of a dirty indicator from storage and to treat the block of memory associated therewith as dirtied if at least one of the redundant copies of the dirty indicator has the predetermined state (abstract, dirty bits on Dtag reads on this limitation).

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3-10 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bannon et al. (Bannon) U.S. Patent No. 5,987,544 in view of Garnett U.S. Patent No. 5,991,900.

As to claim 3, Bannon discloses the invention as claimed in the above, however, Bannon does not specifically disclose the control logic is operable to cause the block of memory associated with a dirty indicator for which at least one copy thereof has the predetermined state to be copied from the main memory to another memory.

Garnett discloses the control logic is operable to cause the block of memory associated with a dirty indicator for which at least one copy thereof has the predetermined state to be copied from the main memory to another memory (col. 22 lines 32-48) for the purpose of preventing data loss.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the control logic is operable to cause the block of memory associated with a dirty indicator for which at least one copy thereof has the predetermined state to be copied from the main memory to another memory of Garnett into the invention of Bannon for the advantages stated above.

As to claim 4, Bannon and Garnett disclose the invention as claimed in the above. Garnett further discloses the other memory is another main memory (col. 22 lines 33-48).

As to claim 5, Bannon and Garnett disclose the invention as claimed in the above. Garnett further discloses further discloses operable to reset each of the redundant copies of a dirty indicator to a state other than the predetermined state after reading the redundant copies of the dirty indicator (col. 22 lines 26-28).

As to claim 6, Bannon and Garnett disclose the invention as claimed in the above. Garnett further discloses the storage comprises at least two memory units (col. 22 lines 18+) each for storing a redundant set of dirty indicators.

As to claim 7, Bannon and Garnett disclose the invention as claimed in the above. Garnett further discloses the control logic includes comparison logic for each of the memory units for determining whether a copy of the dirty indicator is set to the predetermined state (col. 22 lines 18+, specifically "The dirty RAM can be reset, or cleared when it is read by a processing set" reads on this limitation).

As to claim 8, Bannon and Garnett disclose the invention as claimed in the above. Garnett further discloses the control logic includes output logic responsive to the output of each comparison logic for determining whether a block of memory associated with a dirty indicator is to be treated as dirtied (col. 22 lines 18+).

As to claim 9, Bannon and Garnett disclose the invention as claimed in the above. Garnett further discloses each dirty indicator comprises a single bit (col. 22 lines 18+, bit map).

As to claim 10, Bannon and Garnett disclose the invention as claimed in the above. Garnett further discloses a block of main memory is a page of main memory (col. 22 lines 18+).

As to claim 13, Bannon and Garnett disclose the invention as claimed in the above. Garnett further discloses a plurality of processing sets that each includes main memory (col. 22 lines 18+).

As to claim 14, Bannon and Garnett disclose the invention as claimed in the above. Garnett further discloses the processing sets are operable in lockstep, the computer system comprising logic operable to attempt to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error (col. 21 lines 56+).

4. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bannon et al. (Bannon) U.S. Patent No. 5,987,544 in view of Gilham U.S. Patent No. 5,166,883.

As to claim 25, Bannon discloses the invention as claimed in the above, Bannon further discloses redundant copies of the dirty indicator (abstract) however, Bannon

does not specifically disclose wherein, after both redundant copies are read from storage, any difference between the stored redundant copies is considered as indicative of memory corruption.

Gilham discloses wherein, after both redundant copies are read from storage, any difference between the stored redundant copies is considered as indicative of memory corruption (col. 2 lines 66 thru col. 3 lines 16) for the purpose of providing secure retention of data and protecting against corruption of data.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate wherein, after both redundant copies are read from storage, any difference between the stored redundant copies is considered as indicative of memory corruption of Gilham into the invention of Bannon for the advantages stated above.

5. Claims 15-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett U.S. Patent No. 5,991,900 in view of Bannon et al. (Bannon) U.S. Patent No. 5,987,544.

As to claim 15, Garnett discloses a method of managing reinstatement of an equivalent memory state in the main memory of a plurality of processing sets of a fault tolerant computer following a lock step error, wherein a dirty memory subsystem stores copies of dirty indicators that are settable to a predetermined state indicative that a block of main memory associated therewith has been dirtied, the method including the performance of at least one cycle of copying any page of main memory that has been

dirtied from a first processing set to each other processing set, each cycle including reading the redundant copies of a dirty indicator from storage and treating a block of memory associated with the redundant copies as dirtied if all or any one of copy of the dirty indicator has the predetermined state (col. 21 line 55 thru col. 22). However, Garnett does not specifically disclose redundant copies of a dirty indicator.

Bannon discloses redundant copies of a dirty indicator (abstract lines 8-11, "duplicate tag", col. 4 lines 42-47, and col. 6 lines 46-49, "two identical copies" read on this limitation) for the purpose of preventing data loss.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate redundant copies of dirty indicators of Bannon into the invention of Garnett for the advantages stated above.

As to claim 16, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses a block of memory associated with the dirty indicator for which at least one copy has the predetermined state is copied from the main memory to another memory (col. 22 lines 18+).

As to claim 17, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses the other memory is another main memory (col. 22 lines 18+).

As to claim 18, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses each of the redundant copies of the dirty indicator are reset to a state other than the predetermined state after reading the redundant copies of the dirty indicator (col. 22 lines 18+).

As to claim 19, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses maintaining at least two copies of a dirty indicator in at least two memory units (col. 22 lines 18+).

As to claim 20, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses separately assessing the state of copies of a dirty indicator for each of the memory units for determining whether a dirty indicator is set to the predetermined state (col. 22 lines 18+).

As to claim 21, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses responding to each assessment and determining that the block of memory is dirty if any assessment indicates that the dirty indicator has the predetermined state (col. 22 lines 18+).

As to claim 22, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses each dirty indicator comprises a single bit (col. 22 lines 18+, dirty bit map).

As to claim 23, Garnett and Bannon disclose the invention as claimed in the above. Garnett further discloses a block of main memory is a page of main memory (col. 22 lines 18+).

6. Claim 11 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Bannon et al. (Bannon) U.S. Patent No. 5,987,544 in view of Watt U.S. Patent No. 6,272,033.

As to claim 11, Bannon discloses the invention as claimed in the above; however, Bannon does not specifically disclose a hierarchical dirty memory. Watt discloses a hierarchical dirty memory (col. 2 lines 12-27) for the purpose of reducing status processing time (col. 2 lines 19-22).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a hierarchical dirty memory of Watt into the invention of Bannon for the advantages stated above.

7. Claim 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett U.S. Patent No. 5,991,900 in view of Bannon et al. (Bannon) U.S. Patent No. 5,987,544 and further in view of Watt U.S. Patent No. 6,272,033.

As to claim 24, Garnett and Bannon discloses the invention as claimed in the above, however, neither Garnett nor Bannon specifically discloses a hierarchical dirty

memory. Watt discloses a hierarchical dirty memory (col. 2 lines 12-27) for the purpose of reducing status processing time (col. 2 lines 19-22).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a hierarchical dirty memory of Watt into the combined invention of Garnett and Bannon for the advantages stated above.

Response to Arguments

8. Applicant's arguments filed 8/19/04 have been fully considered but they are not persuasive.

In response to applicant's argument on pages 6-8 that the prior arts do not disclose a control logic operable to read the redundant copies of a dirty indicator from storage and to treat the block of memory associated therewith as dirtied if at least one of the redundant copies of the dirty indicator has the predetermined state has been fully considered but it is not persuasive.

Bannon discloses a control logic (Fig. 2 Ref 15a) operable to read the redundant copies (Fig. 2 ref. 28) of a dirty indicator (abstract lines 8-11, "duplicate tag", col. 4 lines 42-47, and col. 6 lines 46-49, "two identical copies" read o this limitation) from storage and to treat the block of memory associated therewith as dirtied if at least one of the redundant copies of the dirty indicator has the predetermined state (abstract, dirty bits on Dtag reads on this limitation).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

1. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

2. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is 571-272-4181. The examiner can normally be reached on M-F 9:00 to 6:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on 571-282-4182. The fax phone number for the organization where this

application or proceeding is assigned is 703-872-9306.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
(703) 872-9306

HK
Primary Patent Examiner
November 28, 2004